Programming the latest FPGA: towards the ALICE 3 readout feasibility study

Project description:
The project entails processing data from an arbitrary source and applying moving average filter with multiple taps on it. The implementation will be done using HDL. It must be demonstrated that it could work on any Xilinx FPGA. The following must be addressed in the projects for the FPGA:

- What is the highest speed of data it can handle?
- How to validating the design? Think and work on a test procedure as well.

The use of LLMs like chatGPT or Bard are encouraged.

The project forms part of the ALICE upgrade at the CERN Large Hadron Collider (https://home.cern/science/accelerators/large-hadron-collider). The work is performed in an international collaboration involving South African institutions and CERN.

Requirements:
Degree level: Electrical Engineering
Minimum Average Pass mark: equal or greater than 65%
Knowledge in electronics, particularly embedded system
Skill: Candidate with knowledge of HDL programming or keen to learn HDL
Highly recommended: The candidate should like a challenge, keen to learn and can work under pressure

Funding:
Candidates are encouraged to source funding via SA-CERN Programme Excellence MSc/PhD Bursary (https://sa-cern.tlabs.ac.za/bursary/).